Embedded Systems Programming

PCIe – An Introduction (Module 11)

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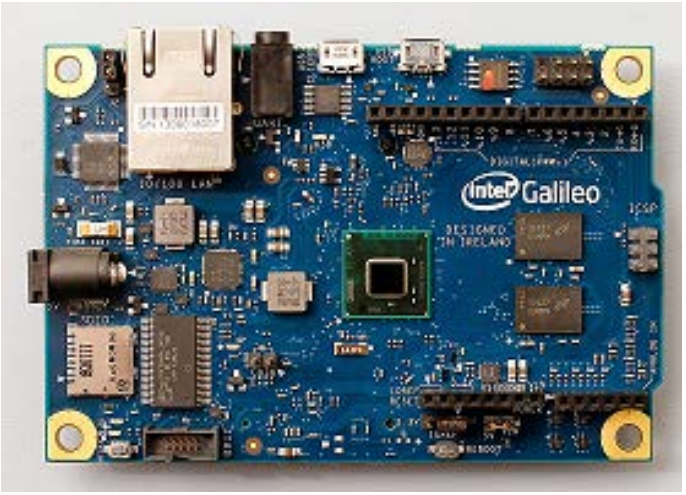
Summer 2014

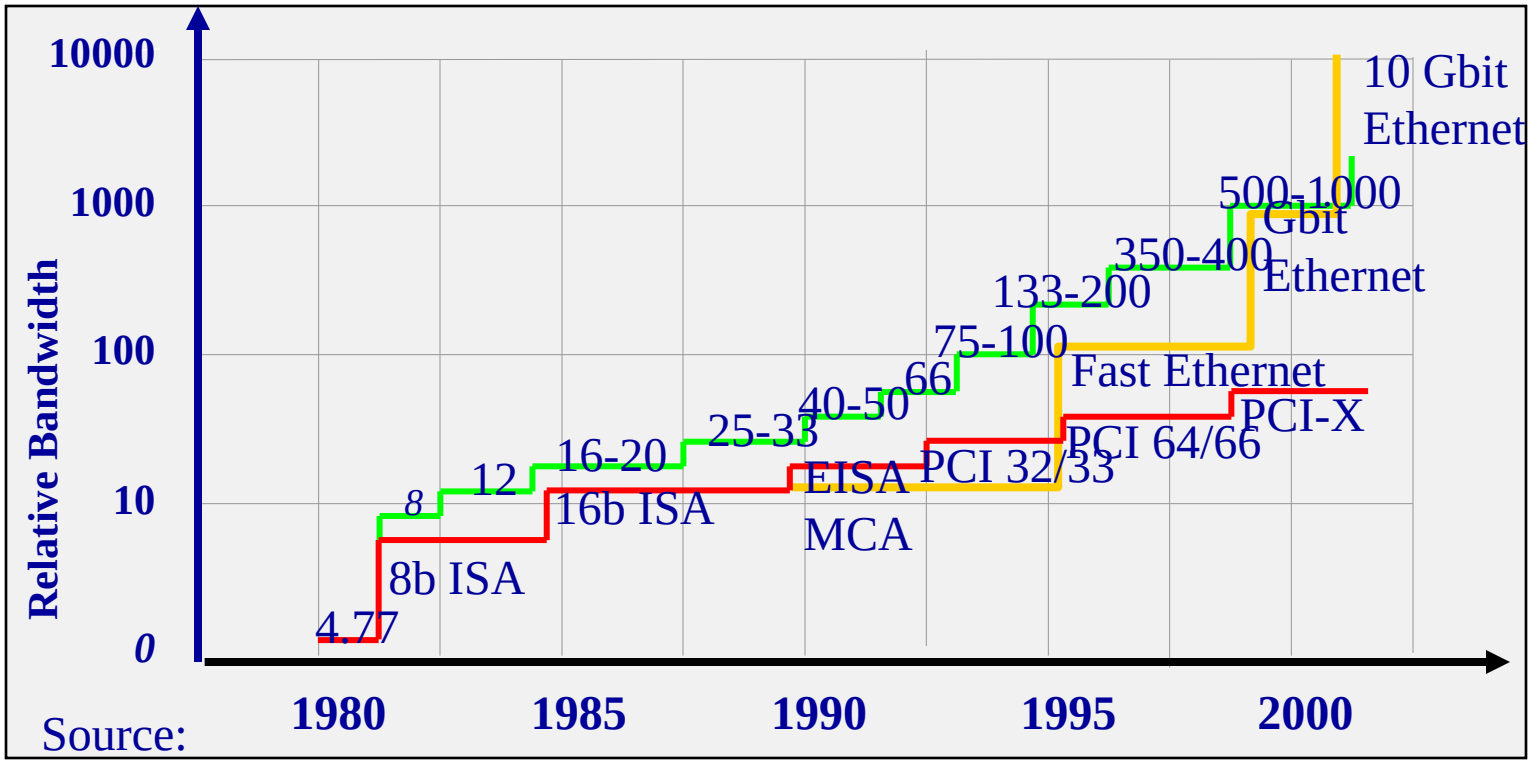


PCI Challenges

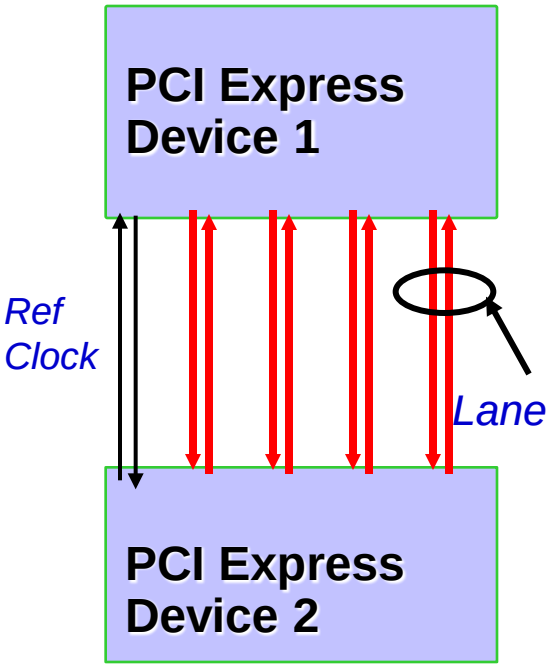
- **Limited Bandwidth**
  - PCI-X and Advanced Graphics Port (AGP) for higher frequency
  - Reduction of distance
- **Bandwidth shared between all devices**
- **Limited host pin-count**
- **Lack of support for real time data transfer**
- **Stringent routing rules**
- **Lack of scaling with frequency and voltage**
- **Absence of power management**
- **PCI-X -- an enhancement of the 32-bit PCI Local Bus for a higher bandwidth demand.**
  - a double-wide version of PCI, running at up to four times the clock speed

Inter-Networking Driving Demand

- Multimedia applications drive the need for fast, efficient processing of data over wired or wireless media
- CPU performance doubles about every 18 months while PC Bus performance doubles about every 3 years



PCI Express Basics



x4 Link Example

- Serial, point-to-point, Low Voltage Differential Signaling
- 2.5GHz full duplex lanes (2.5Gb/s)
  - PCIe Gen 2 = 5Gb/s
- Scaleable links – x1, x4, x8, x16
- Packet based transaction protocol
- Software compatible but with higher speeds
- Built-in Quality of Service provisions
  - Virtual Channels
  - Traffic Classes
- Reliability, Availability and Serviceability
  - End-to-End CRC (Cyclic redundant checking)
  - Poison Packet
  - Native Hot Plug support
- Flow Control and advance error reporting

PCI Express Performance

Link Width	X1	X2	X4	X8	X12	X16	x32
Bandwidth in Gbits/s (Tx and Rx)	5	10	20	40	60	80	160
Throughput in GB/s (Tx and Rx)	.5	1	2	4	6	8	16
Throughput in GB/s (per direction)	.25	.5	1	2	3	4	8

Raw: Assuming 100% efficiency with no payload overhead.

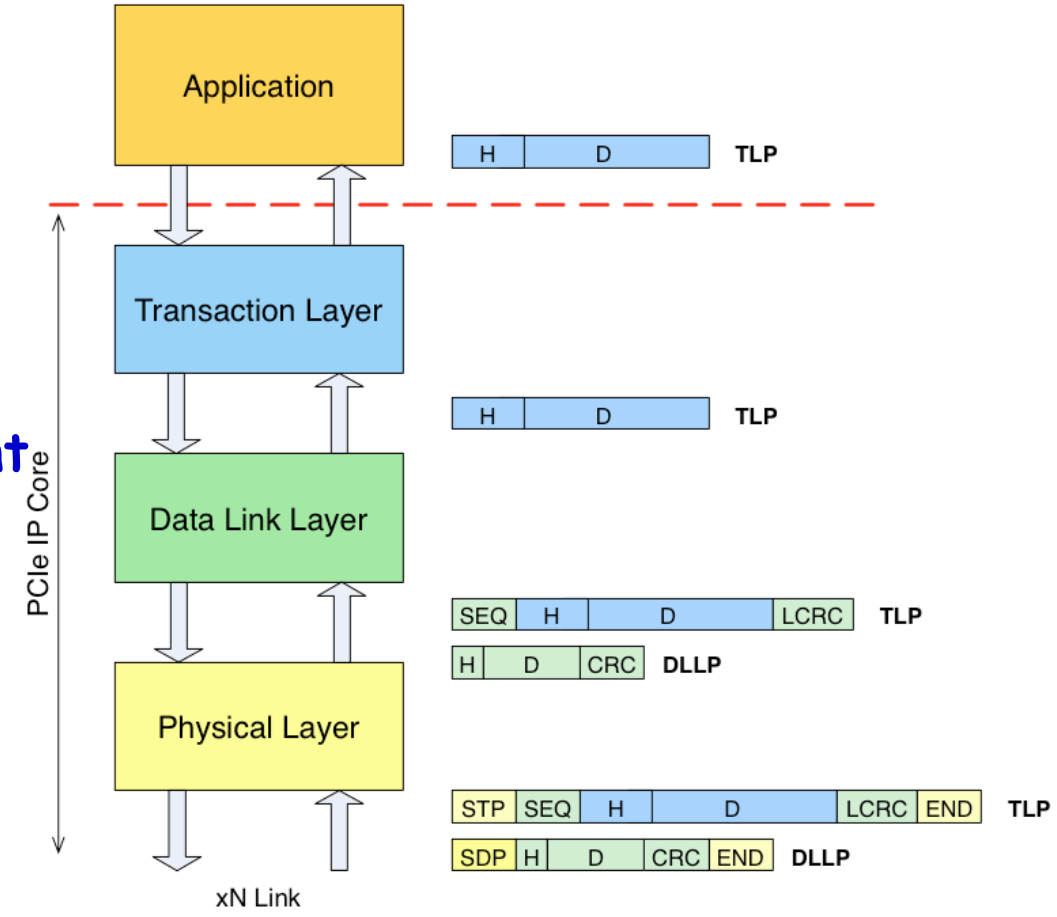
= PCI 32/66

= PCI or PCI-X 64/66

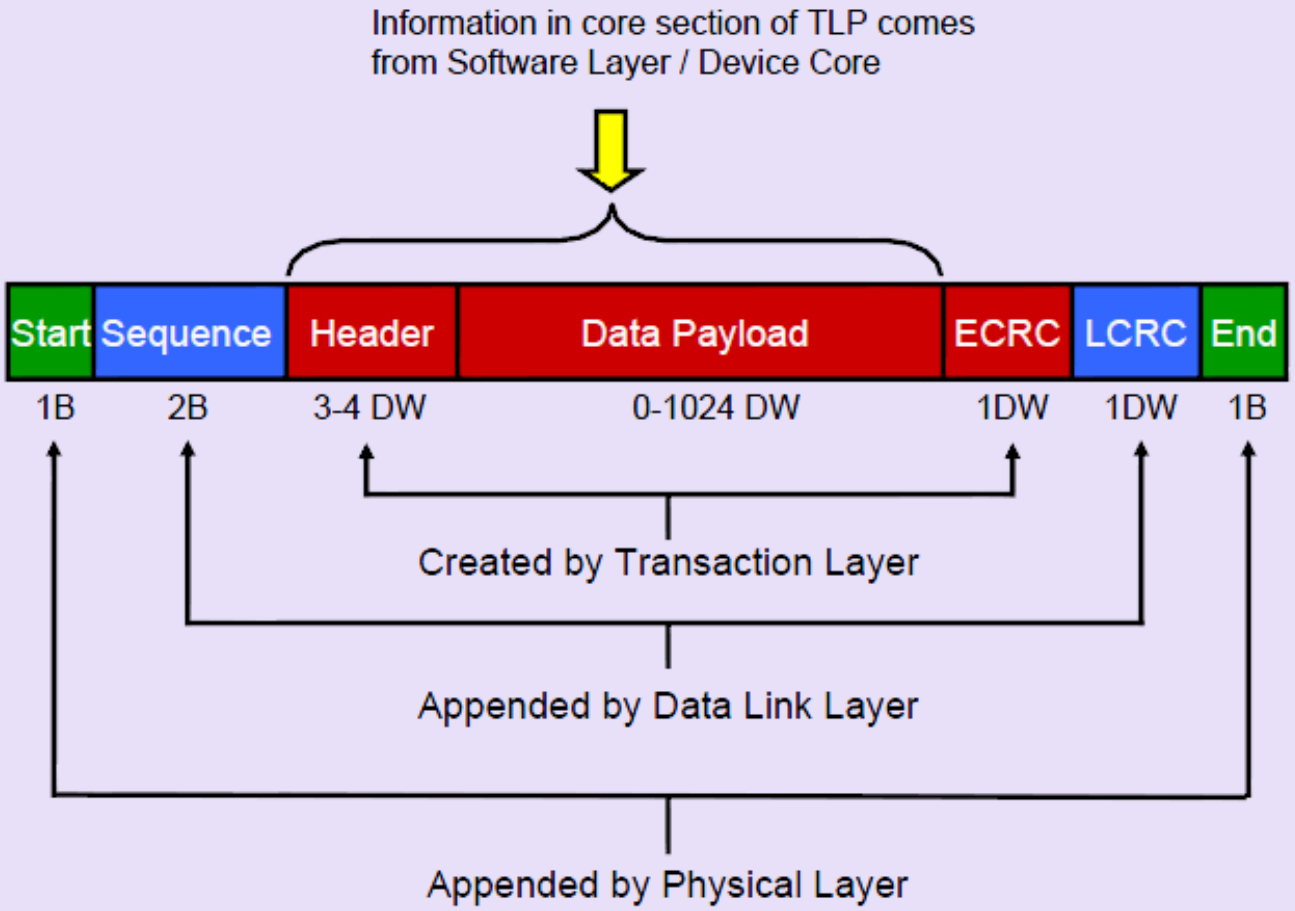
= PCI-X 64/133

PCIe Layers

- Layered architecture
- Application Data transferred via packets
  - Transaction Layer Packet (TLP)
- PCIe core usually implement the lower three layers
- Protocol handling
  - connection establishing
  - link control
  - flow control
  - power management
  - error detection and reporting



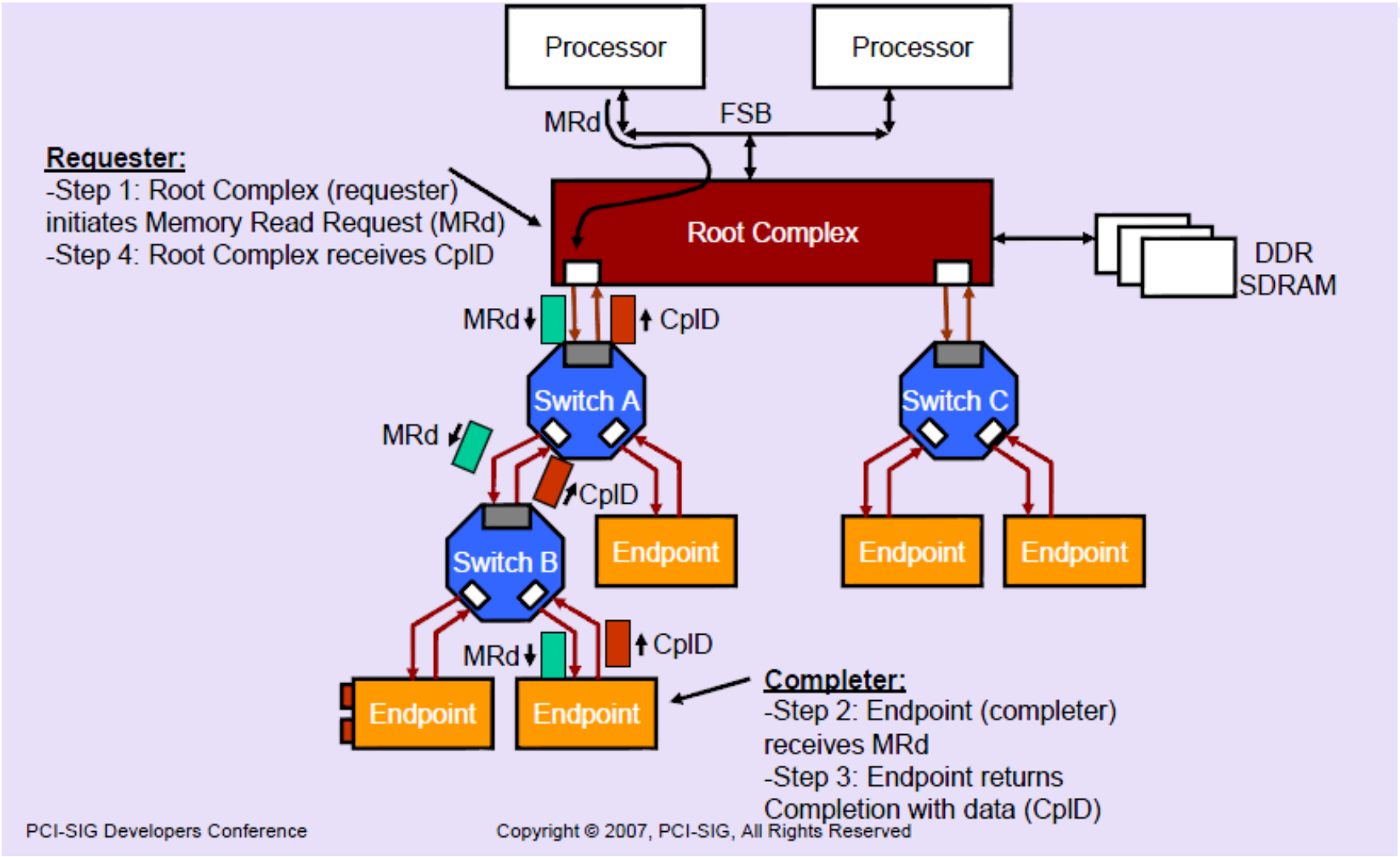
PCIe TLP Structure



Transaction Types, Address Spaces

- **Request are translated to one of four transaction types by the Transaction Layer:**
  - Memory Read or Memory Write. Used to transfer data from or to a memory mapped location
    - also supports a *locked memory read transaction variant.*
  - I/O Read or I/O Write. Used to transfer data from or to an I/O location
    - restricted to supporting legacy endpoint devices.
  - Configuration Read or Configuration Write – Used to discover device capabilities, program features, and check status in the 4KB PCI Express configuration space.
  - Messages. Handled like posted writes. Used for event signaling and general purpose messaging.

Programmed I/O Transaction



Supplementary Slides

Transaction Layer Packet Types

Description	Abbreviated Name
Memory Read Request	MRd
Memory Read Request – Locked Access	MRdLk
Memory Write Request	MWr
IO Read Request	IORd
IO Write Request	IOWr
Configuration Read Request Type 0 and Type 1	CfgRd0, CfgRd1
Configuration Write Request Type 0 and Type 1	CfgWr0, CfgWr1
Message Request without Data Payload	Msg
Message Request with Data Payload	MsgD
Completion without Data (used for IO, configuration write completions and read completion with error completion status)	Cpl
Completion with Data (used for memory, IO and configuration read completions)	CplD
Completion for Locked Memory Read without Data (used for error status)	CplLk
Completion for Locked Memory Read with Data	CplDLk