Embedded Systems Programming

Quark SOC and Galileo
(Module 7)

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Current Processor Design

- Moore’s law continues to hold true, transistor counts doubling every 18 months
  - But can no longer rely upon increasing clock rates and instruction-level parallelism to meet computing performance demands

- Semiconductor device fabrication process

- How to best exploit ever-increasing on-chip transistor counts?
  - Multi- & many-core (MC) devices are new technology wave
  - exploiting explicit parallelism in the new devices

- Size and Power constraints
Intel Processors

- **X86 32/64 architecture**
  - 486 – first pipelined x86 design
  - Pentium – the first x86 superscalar CPU

- **Processors for**
  - Server (Xeon), desktop (Core i3/i5/i7), mobile (Core i3/i5/i7), and embedded (Atom)
  - All of them support hypervisor (VM)

- **Differences**
  - CPUs, memory, and interconnection bandwidth
  - reliability (quality of dies) and form factor
  - power and thermal requirements

- **Uses available clock cycles and power, not to push up higher clock speeds and energy needs**
Galileo Board

- 400MHz Quark SoC
- 256MB DDR3
- Ethernet
- USB Host Port
- MicroSD Support
- I2C, SPI Support
- PCI Express Mini Cards
- Serial Connectivity
- GPIO
- Linux on Board

Intel Quark SoC X1000.

- **SOC** -
  - CPU core (x86)
  - cache, internal memory (flash, SRAM)
  - IO interfaces and external buses
  - interconnection or switches
  - misc (clock, JTAG)

- **Chip size, power and pins**
  - 32nm process in 1st Quark
  - one-fifth the size and one-tenth the power of low-end Atom chip
  - 393 solder balls on 15mm²
  - 5 power rails (3.3V, 1.8V, 1.5V, 1.05V, 1.0V)
Quark Core Internal Architecture

- 32-bit RISC integer core
- Single cycle execution
- Instruction pipelining
- Floating-point unit
- Cache with cache consistency support (16-Kbyte for both data and instructions)
- Memory management unit

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Pins in Quark

- **Example:** High Speed UART Interface, SIU1_RDX SIU1_TXD

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Dir</th>
<th>Term</th>
<th>Power</th>
<th>Type</th>
<th>S4/S5</th>
<th>S3</th>
<th>Reset</th>
<th>Enter S0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIU0_RXD</td>
<td>I</td>
<td>20k(H)</td>
<td>3.3V</td>
<td>CMOS3.3</td>
<td>Off</td>
<td>Off</td>
<td>Pull-up</td>
<td>Pull-up</td>
</tr>
<tr>
<td>SIU0_TXD</td>
<td>O</td>
<td>-</td>
<td>3.3V</td>
<td>CMOS3.3</td>
<td>Off</td>
<td>Off</td>
<td>VOH</td>
<td>VOH</td>
</tr>
</tbody>
</table>

- **Six different power states**
  - S0 - the system is completely powered ON and fully operational
  - S5 - the system is completely powered OFF
  - S1, S2, S3 and S4 - sleeping states, the system appears OFF because of low power consumption and retains enough of the hardware context to return to the working state

- **In Galileo schematics**

TXD OUTPUT FROM QUARK

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**IO Expander and GPIO Multiplexing**

- **CY8C9540A – I2C interfaced expander**
  - with 40 I/O data pins (ports 0-5) independently configurable as inputs, outputs, bi-directional input/outputs, or PWM outputs

- To configure a pin
  - an I2C control message to the chip which includes a register address